CORE-1553 & CORE-MMSI

MIL-STD-1553 and MMSI/EBR-1553 Protocol Cores for Programmable Logic Devices

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Contact Information

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Glossary of Terms

CORE-1553 -	MIL-STD-1553B Intellectual Property Product from Condor Engineering
CORE-MMSI -	MMSI/EBR-1553 Intellectual Property Product from Condor Engineering
BC -	Bus Controller
RT -	Remote Terminal
BM -	Bus Monitor
PLD -	Programmable Logic Device (Same as FPGA) - Chip
FPGA -	Field Programmable Gate Array (Same as PLD) - Chip
MMSI -	Miniature Mission Stores Interface (10 MHz 1553 using RS-485)
BIT -	Built-in-Test
MMU -	Memory Management Unit (Extended memory addressing)
nsec -	nanosecond
µsec -	microsecond
msec -	millisecond
Instantiation -	A single instance of a core that is synthesized or combined with other logic and then synthesized, and loaded into a single programmable logic device, volatile or non-volatile memory, other programmable devices or ASIC.

Introduction

By taking advantage of the revolutionary advances in capacity, performance and cost-effectiveness of a new generation of programmable logic devices (PLDs), Condor Engineering's CORE-1553 and CORE-MMSI products provide military system designers with new and exciting protocol communications options. The military electronics industry is now rapidly moving to deploy the higher levels of integration provided by System on a Chip (SoC) or integrated I/O implementations. This integration can bring dramatic benefits of lowered costs, reduced chip counts and increased MTBF for both PLD and ASIC designs. Condor's CORE products provide those benefits, along with significant new features that offer expanded options for increased deployed system functionality.

CORE-1553 and CORE-MMSI are the industry's first 1553/MMSI downloadable (or "soft") encoder/decoder/processing cores that can provide one or more, dual redundant military protocol channels when loaded onto a single Programmable Logic Device (PLD), Field Programmable Gate Array (FPGA) chip or ASIC device. Utilizing a custom, high performance RISC processor, Condor's CORE-1553 product is a uniquely portable and flexible solution for the entire range of MIL-STD-1553 implementations, including MIL-STD-1760 and Link-16.

Condor's CORE-MMSI product supports the emerging MMSI/EBR-1553 bus and is nearly identical in functionality to 1553B, but runs at a faster 10 MHz rate over RS-485.

Benefits

Obsolescence Management

Parts obsolescence is a major risk for all multi-year electronics production projects. This risk can be reduced with Condor CORE-1553/MMSI downloadable cores. Designers are not tied to one specific part – or even one manufacturer of PLD/FPGAs. This is in contrast to sole source, specialized protocol ASICs and processors (as well as their manufacturing methods), which could be discontinued at any time. It is a strategic design feature that CORE-1553/MMSI can migrate to new FPGA/PLD parts while maintaining complete functional compatibility.

Reduced Footprint & Higher Reliability

Combining multiple 1553 channels and other functions, including processors, I/O and even a PCI interface into a single part will significantly reduce part count, board space and thermal loading, resulting in higher reliability. Reduced part counts can also result in lower system power requirements.

Cost Reduction

Production and life cycle costs will drop with time as a result of implementing FPGA/PLD cores. FPGA/PLD prices have an established history of significantly dropping over time, while small market ASIC product pricing trends upward, or at best stays constant (see CORE-1553 vs. ASIC chart). Also, with common development tools, iteration flexibility and most significantly – integrating multiple board functions within a single FPGA/PLD component, CORE products can help reduce overall costs even further.

Better Reliability, Lower Power Consumption and Less Weight

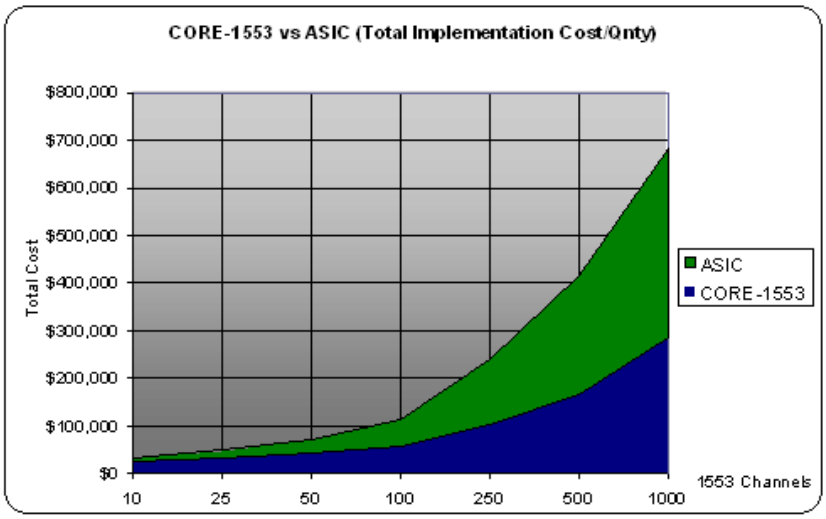
Combining several board level functions onto a single PLD part can result in increased MTBF values, decreased power consumption and reduced weight.

Advanced Feature Set

CORE-1553 intellectual property products are available with either Individual-function (separate cores available for Bus Controller, single Remote Terminal, multiple Remote Terminal or Bus Monitor) or Full Multi-function (a single core for 1553 with simultaneous Bus Controller, multiple Remote Terminals and Bus Monitor) operational modes for your avionics subsystem. CORE-MMSI products are only available in individual-function configurations. All 1553/MMSI signal level decoding, encoding, message processing, buffering and protocol validation/legalization is provided by Condor's CORE-1553 and CORE-MMSI products, and when combined with compliant transceivers and transformers gives system designers complete 1553/MMSI solutions. The Full Multi-function 1553 product offers features previously found only on board level products. Multiple levels of Built-In-Test are available to add new levels of system assurance.

Low Risk

A simple memory map inter-connect design allows CORE-1553/MMSI to be quickly integrated into most processor memory bus and backplane (i.e. PCI) subsystem designs. CORE-1553 is the same technology as utilized on Condor Engineering's extensive line of proven and industry-leading board level products for VME, PCI, cPCI, PMC, PCMCIA and PC/104 platforms.



This chart reflects relative costs by comparing protocol ASIC prices against CORE-1553 license and Integration Kit expense. Many programs may find even greater savings as the cost of the PLD part may significantly fall over the system life cycle.

CORE-1553/MMSI Product Summary

Standard Products

CORE-1553
- Individual-function
  - Bus Controller
  - Single Remote Terminal
  - Multiple Remote Terminal
  - Bus Monitor
- Full Multi-function
  - Simultaneous Bus Controller, 31 Remote Terminals and Bus Monitor

CORE-MMSI
- Bus Controller
- Single Remote Terminal

These six CORE-1553 and CORE-MMSI products are supplied as separate Integration Kits, each for a single development station. Each Integration Kit contains a software CD, documentation, ten embedded system licenses and one year of maintenance/support. Continued maintenance/support requires an annual follow-on contract. Additional development seats, embedded system licenses and extended maintenance/support are available.

Individual-Function Products

Separate, individual-function, CORE-1553 products are available for Bus Controller (BC), single Remote Terminal (RT), multiple RT (mRT) and Bus Monitor (BM) operational modes. Separate, individual-function CORE-MMSI products are available for Bus Controller (BC) and single Remote Terminal (RT) operational modes. Bus Controller and single Remote Terminal individual-function products are available for CORE-MMSI. Individual-function products require the least amount of PLD/FPGA resources. CORE-1553 BC and RT cores include a simultaneous, sequential, basic Bus Monitor (bBM) functionality that provides decoded words, valid/invalid indication, and 48-bit time tags.

Individual-function products may be contained wholly within a single PLD – including data structure memory. Individual-function products are specifically targeted for embedded applications where core size and board space are paramount.

Data structure memory may be implemented internally to the PLD (sufficient internal RAM space required), or externally (specific RAM interfaces not included).

Full Multi-Function CORE-1553 Product

The full multi-function CORE-1553 product is a single, tightly coupled core that provides simultaneous Bus Controller, multiple Remote Terminals and Bus Monitor operational modes. PLD requirements are greater than those of Individual-function CORE products.

Simultaneous, sequential bus monitor functionality that provides decoded words, valid/invalid indication, and time tagging is also included. Contact Condor about future optional Health Diagnostics Monitor (HM).

Data structure memory may be implemented internally to the PLD (sufficient internal RAM space required), or externally (specific RAM interfaces not included).

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Features and PLD Resource Requirements:

CORE-1553/MMSI Basic Features	1553	MMSI
Protocol Support		
MIL-STD-1553B, Notice 2 Functionality	Std	-
MMSI-EBR Compliant - Star Topology	-	Std
MMSI Link-mode	-	Std
MIL-STD-1760 Start-up-time compliant	Std	-
MIL-STD-1760 Start-up with Busy Bit	Std	-

Typical CORE PLD/FPGA Requirements	Individual	Multi-function
Internal RAM (minimum)	84 Kbits	148 Kbits
Logical Elements (1 flip-flop; 4 input look-up)	2800	3200
64 pins (minimum)	Std	Std
80 MHz input Clock	Std	Std
1 Mbyte Data Structure addressability	Std	Std

General CORE-1553/MMSI Features	Individual	Multi-Function
General		
HB-16 Processor	Std	Std
Power On Self Test, Periodic BIT, Initiated BIT	Std	Std
Host Interrupt Line	Std	Std
1 MHz Encoder/Decoder	1553	1553
10 MHz Encoder/Decoder	MMSI	-
Message Time Stamping		
48 bit Time Stamp	Std	Std
Time Tag Clear to Zero Command	Std	Std
Data Structure RAM Sizes		
1 Kbyte to 16 Mbyte data structure memory	Std	Std
Data Structure RAM Addressing		
Internal RAM	Std	Std
External RAM Interface	Std	Std
23 lines addressing	Std	Std
RT Address Line, Auto-Parity Validation	Std	Std
Functions controlled thru RAM & Registers	Std	Std
Buffer Structure Methods		
Link List	Std	Std
Ping-Pong	Std	Std
Circular	Std	Std
Shareable data buffers	Std	Std
On-the-fly Modifications		
Set-up	Std	Std
Data Structures	Std	Std
Messages	Std	Std

PLD Suggestions

Condor Engineering, Inc. suggests the following PLD and FPGA devices:

Xilinx

Virtex II family
Virtex II 2V250 -5 Speed
Individual-function CORE-1553
Individual-function CORE-MMSI
Virtex II 2V1000 -5 Speed
Individual-function CORE-1553,
Individual-function CORE-MMSI,
Full multi-function CORE-1553,
Full multi-function CORE-MMSI,
Multiple Individual-function CORE.

Altera

Stratix family -6 Speed
Individual-function CORE-1553
Full multi-function CORE-1553
Multiple Individual-function 1553 Cores

CORE Product Typical PLD Resource Requirements

Example #1: 1553 Remote Terminal, Xilinx Virtex II, XST synthesis, internal RAM
Number of Slices: 1351
Number of Slice Flip Flops: 962
Number of 4 input LUTs: 2045
Number of Block RAMs: 14

Example #2: MMSI Bus Controller, Xilinx Virtex II, XST synthesis, 32KB internal RAM
Number of Slices: 1372
Number of Slice Flip Flops: 941
Number of 4 input LUTs: 2090
Number of Block RAMs: 23

Bus Controller Features

Multiple Messaging Methods
- Frame Scheduling
- "One-Shot" Operations
- 1553 Message Types Supported
  - BC->RT, RT->BC, RT->RT, Mode Code, Broadcast

Full Error Detection/Invalid Message Reporting
- No-Response Report
- Invalid Message Notification
- Late Message Arrival Report
- RT Time-out Report
- Error Indicator Bits

Message Level Automatic Retries
- Programmable for same/alternate buses
- 1 to 8 retries on same/alternate buses (1553 only)

Time Tags, Data Words and Status Words
- All BC Buffers are Time Tagged
- All Valid Data Words are Stored
- All Valid Status Words are Stored

Intermessage Gap Time Control
- Programmable 4 - 65,000 usecs per message & Programmable Defaults
- Supports 1553 4 µsec IGT

Multiple Data Buffering Techniques
- Single Buffers
- Multiple Message Buffers

Advanced Message Scheduling
- Multiple Message Buffers
- Start-up Frames

MMSI Features
- 31 RTs Supported
- Composite BM Out

MMSI Modes
- EBR-1553 Specification Compliant
- Link-mode Compliant

Remote Terminal Features

Remote Terminal Features CORE-1553/MMSI	Single RT	Multiple RT
General		
Single RT Support	Std	Std
Full 31 RT, 30 SA (memory dependent)	-	Std
Autoprogram RT Address	Std	-
External RT Address Verification	Std	Std
RT Response Time		
Programmable RT Minimum Response Time	Std	Std
Message Time Tagging		
48 bit Time Tag	Std	Std
Message Legalization		
RT/ T-R/ SA/ WC/ MC Legalization	Std	Std
SA31 Mode Code Selectable	Std	Std
Broadcast Selection	Std	Std
Full Message Error Reporting	Std	Std
Mode Code Support		
All Mode Codes Supported	Std	Std
Mode Code Processing	Std	Std
Reserved Mode Codes	Std	Std
Data Structures		
RT Multiple Message Buffers		
Receive Data Buffers	Std	Std
Transmit Data Buffers	Std	Std
Mode Code Data Buffers	Std	Std
Broadcast Data Buffer	Std	Std
RT Control Buffer	Std	Std
RT Wrap with settable return address	Std	Std

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Bus Monitoring Features

Basic BM Features

All Word-based bus activity

Message Buffer Time Tagging
- Beginning of Message Time
- Gap Time
- RT Response Time

Full Error Detection and Reporting
- Invalid Word
- Late Response
- No Response
- Early Response
- Inter-message Gap
- High Word
- Low Word
- Incorrect RT Address
- Inverted Sync
- Parity Error
- Manchester
- Word Gap

Built-In-Test Functionality

Embedded systems need to demonstrate a high level of system operational assurance. To meet this requirement, all CORE-1553 and CORE-MMSI products provide three powerful Built-In-Tests (BIT), a General Health Status Register, as well as wrap-around testing.

- **Power On Self Test (POST)**

  Comprehensive Power-On self test that verifies the operational status of all processor instructions, performs a RAM test, and verifies encoder/decoder operation within 75 msecs after power-up.

- **Initiated BIT (IBIT)**

  Comparable to the POST, but performs only a minimal RAM test (because a RAM test would overwrite application data and require re-initialization of that data). Initiated by programmable command or by Mode Code. IBIT maintains interoperability with normal operational functions.

- **Periodic BIT (PBIT)**

  PBIT is a subset of the POST that is self-initiated at no less than 100 msec intervals. PBIT tests subset functionality across all parts of the system without interfering with normal operational functionality.

- **Internal Wrap**

  The host application can programmatically select an internal wrap connection for application testing.

- **External Cable (A-B Bus Loop Test) Wrap**

  With addition of an external connection between A and B buses at the end of a cable, signal continuity and transceiver function can be tested. Available only for 1553.

Built-In-Test Features

Bit Test Operations	POST	IBIT	PBIT
Start BIT Testing			
Initiated at Start-up	Std	-	-
Host Initiated	-	Std	-
Mode Code Initiated	-	Std	-
Self Initiated	-	-	Std
BIT In-Progress			
In-Progress Bit Set, Register	Std	Std	Std
Result Registers Set	Std	Std	Std
Results Cleared	Std	Manual	Manual
Processor Check			
Instruction fetch	Std	Std	Std
Processor data paths	Std	Std	Std
Instruction decoder	Std	Std	Std
Conditional branches	Std	Std	Std
Stack Operations	Std	Std	Std
RAM Test			
RAM Test	Std	-	-
Reduced RAM Test	-	Std	Std
Four Multi-bit Patterns	Std	-	-
Parity	Option	Option	Option
Encoder/Decoder Wrap			
Unique Values	Std	Std	-
Fail-safe timer	Std	Std	-
Time tag Counter Verification	Std	Std	Std
Posting BIT Results			
Sub-set Test Results Posted	Std	Std	Std
In-progress Bit Cleared	Std	Std	Std
Error Operations			
Inhibit Operation upon Error	Std	-	-
Terminal Fail Set, Status Word	Std	Std	Std
BIT Fail Register bit Set	Std	Std	Std
BIT Time Values			
Completion time in msec	≤ 75*	≤ 25	≤ 25
Repeat Rate in msec	-	-	≤ 100
General Health Status Register			
Always available	Std	Std	Std
Processor Failure if stopped	Std	Std	Std

* All BIT is completed within 1553 required time frames.
Busy Bit in the Status Word need not be set.

Development and Support Packages

Condor's CORE-1553/MMSI products consist of several elements - an Integration Kit, annual Maintenance & Support and Embedded System Licenses. CORE-1553 and CORE-MMSI products are licensed under a specific Technology License Agreement. Contact Condor about specialized 1553 variations such as B-2, Euro Fighter, 1760, Link-16, etc.

Integration Kit

CORE-1553 or CORE-MMSI Integration Kits (single development seat), when combined with your design/synthesis tools, include everything required to get your development started - software, documentation, examples, support and several Embedded System Licenses. Integration Kit software may only be installed on a single workstation at any time.

Maintenance and Support

Each Integration Kit includes one year of technical support (single point of contact), and one year of web-delivered updates. Follow-on annual maintenance/support packages are available.

Product Licenses

Each Integration Kit contains ten Embedded System Licenses (each license represents a single instantiation of the embedded CORE program). A separate Embedded System License is required for each CORE instantiation whether inside an embedded part or on an emulation/simulation system. Additional CORE-1553 and CORE-MMSI Embedded System Licenses are available with quantity level discounts. Once assigned to a programmed part, license(s) are considered to be part of the circuit assembly. The embedded program may be "soft" updated, but the license(s) may not be re-assigned to another programmed part.

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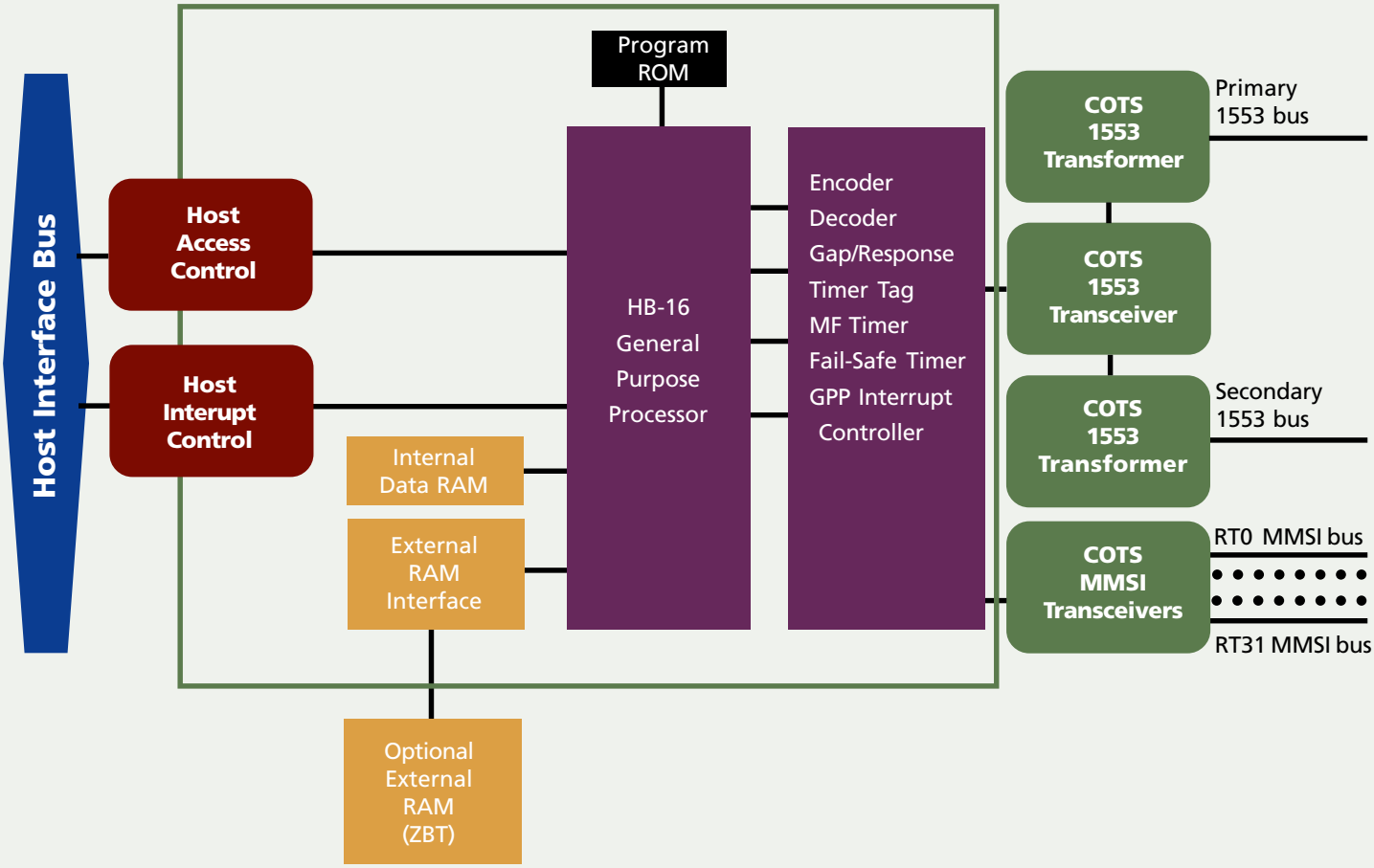
CORE-1553/MMSI Architecture Overview

The engine of Condor's CORE products is a high performance, small gate-count RISC processor, the Humming-bird©-16 (HB-16). This processor was specifically designed to meet the integer level bit shifting, word level encoding, decoding and buffering requirements of network protocols such as 1553, MMSI and others. The HB-16 processor is programmed in C and can be tailored for specialized network requirements and to match various ASIC data structures.

1553 or MMSI functions are accessed via programmable control registers or memory mapped data structures (located in internal PLD or external RAM), for all BC, RT and Monitor functions. For almost all CORE-1553/MMSI implementations, the PLD designer will not need to know the details of how CORE-1553/MMSI internally operates. Users with specialized applications should contact Condor about possible modifications to internal HB-16 programming. HB-16 programming is stored in local PLD PROM or off-chip PROM/memory, and is auto- loaded when the PLD powers-up/resets (the system designer selects where this instruction memory/CORE load is stored).

Contact Condor for information on multiple channel implementations and other specific requirements.

CORE-1553 Architecture Objects



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